UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/834,276	04/12/2001	Roger Lewis	H26651	4922

128 7590 05/17/2004

HONEYWELL INTERNATIONAL INC.
101 COLUMBIA ROAD
P O BOX 2245
MORRISTOWN, NJ 07962-2245

EXAMINER	
SHAPIRO, LEONID	

ART UNIT	PAPER NUMBER
2673	13

DATE MAILED: 05/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/834,276	LEWIS, ROGER	
	Examiner	Art Unit	
	Leonid Shapiro	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,14-19 and 21-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14-19 and 21-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. In view of the Appeal Brief filed on 03-03-04, PROSECUTION IS HEREBY REOPENED. Rules set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 21-23 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The newly introduced limitation " a hardware based pulse width modulator" is not defined in the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, 4-6, 8-9,11-12,14-17,19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zuraski et al. (US Patent No. 5,589,805) in view of Burgan et al. (US Patent 6, 445, 790, B1).

As to claim 1, Zuraski et al. teaches a method for pulse width modulation comprising the steps of: providing a pulse width modulator having n (6) bits of resolution (from Col. 4, Line 61 to Col. 5, Line 8 and Col. 6, Lines 1-10) and nominal time period Pn (See Figs. 1A-B, 3, items Tpwm, 17, in description See Col.3, Lines 32-35, from Col. 3, Line 63 to Col. 4, Line 9 and Col. 5, Lines 1-8); supplying a timer (See Fig 3, item 17, Col. 3, Lines 32-39) to generate K associated states wherein K is equal 2 (See Col. 6, Lines 1-10) and having period Pt (T1 or T2) (See Fig. 1A-B, items T1, T2, in description See Col. 5, Lines 9-27); associating a modulator output value with each one of K states (See Figs. 1A-B, 3, items S, S+1, in description See Col. 5, Lines 9-27); establishing a pulse width modulation update interval (control period Tc in the reference) of K* Pt (Tc = T1+T2) (See Fig. 1A, items Tc, T1, T2, Col. 5, Lines 24-27).

Zuraski et al. does not show an additional timer to generate K associated states, wherein K is greater than 2.

Burgan et al. teaches an additional timer (counter) (See Fig. 11, item 1144, Col. 11, lines 51-65) to generate K associated states, wherein K is greater than 2 (See Fig. 12, items T0-T7, Col.12, Lines 9-18).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement (timer) counter as shown by Burgan et al. in Zuraski et al. apparatus and method in order to create an adaptive pulse-width modulator for pulse-width modulating a digital tone signal (See Col. 3, lines 60-64).

As to claim 5, Zuraski et al. teaches a method for improving the resolution of n-bit pulse width modulator having n (6) bits of resolution (from Col. 4, Line 61 to Col. 5, Line 8 and Col. 6, Lines 1-10) and nominal time period Pn (See Figs. 1A-B, 3, items Tpwm, 17, in description See Col.3, Lines 32-35, from Col. 3, Line 63 to Col. 4, Line 9 and Col. 5, Lines 1-8); supplying a timer (See Fig 3, item 17, Col. 3, Lines 32-39) to generate K associated states wherein K is equal 2 (See Col. 6, Lines 1-10) and timer period Pt (T1 or T2) (See Fig. 1A-B, items T1, T2, in description See Col. 5, Lines 9-27); associating a modulator output value with each one of K states (See Figs. 1A-B, 3, items S, S+1, in description See Col. 5, Lines 9-27); and outputting a pulse according to modulator output value during each time period Pn (Tpwm) occurring within timer period Pt (T1 or T2) during each one of K (2) timer states, whereby the resolution of n bit pulse width modulator equals n + log2(K) or 6 + log2(K) or 7 (See Fig. 1A, items Tc, T1, T2, S, S+1, Col. 5, Lines 8-27 and Col. 6, Lines 1-10).

Zuraski et al. does not show an additional timer to generate K associated states, wherein K is greater than 2.

Burgan et al. teaches an additional timer (counter) (See Fig. 11, item 1144, Col. 11, lines 51-65) to generate K associated states, wherein K is greater than 2 (See Fig. 12, items T0-T7, Col.12, Lines 9-18).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement (timer) counter as shown by Burgan et al. in Zuraski et al. apparatus and method in order to create an adaptive pulse-width modulator for pulse-width modulating a digital tone signal (See Col. 3, lines 60-64).

As to claim 14, Zuraski et al. teaches an apparatus for pulse width modulator comprising: an n (6) pulse width modulator (from Col. 4, Line 61 to Col. 5, Line 8 and Col. 6, Lines 1-10) having a nominal time period Pn (See Figs. 1A-B, 3, items Tpwm, 17, in description See Col.3, Lines 32-35, from Col. 3, Line 63 to Col. 4, Line 9 and Col. 5, Lines 1-8); supplying a timer (See Fig 3, item 17, Col. 3, Lines 32-39) to generate K timer states wherein K is equal 2 (See Col. 6, Lines 1-10) and timer period Pt (T1 or T2) (See Fig. 1A-B, items T1, T2, in description See Col. 5, Lines 9-27); a computing device for assigning a modulator a modulator output value with each one of K states (See Figs. 1A-B, 3, items S, S+1, in description See Col. 5, Lines 9-27); and whereby modulator outputs a plurality of pulses according to modulator output value during each time period Pn (Tpwm) occurring within timer period Pt (T1 or T2) during each one of K (2) timer states, whereby the resolution of n bit pulse width modulator equals n + log2(K) or 6 + log2(K) or 7 (See Fig. 1A, items Tc, T1, T2, S, S+1, Col. 5, Lines 8-27 and Col. 6, Lines 1-10).

Zuraski et al. does not show an additional timer to generate K associated states, wherein K is greater than 2.

Burgan et al. teaches an additional timer (counter) (See Fig. 11, item 1144, Col. 11, lines 51-65) to generate K associated states, wherein K is greater than 2 (See Fig. 12, items T0-T7, Col.12, Lines 9-18).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement (timer) counter as shown by Burgan et al. in Zuraski et al. apparatus and method in order to create an adaptive pulse-width modulator for pulse-width modulating a digital tone signal (See Col. 3, lines 60-64).

As to claim 19, Zuraski et al. teaches an apparatus improving the resolution of n bit pulse width modulator (from Col. 4, Line 61 to Col. 5, Line 8 and Col. 6, Lines 1-10) having a nominal Pn period (See Figs. 1A-B, 3, items Tpwm, 17, in description See Col.3, Lines 32-35, from Col. 3, Line 63 to Col. 4, Line 9 and Col. 5, Lines 1-8), the apparatus comprising: a timer (See Fig 3, item 17, Col. 3, Lines 32-39) to generate K timer states wherein K is equal 2 (See Col. 6, Lines 1-10) and timer period Pt (T1 or T2) (See Fig. 1A-B, items T1, T2, in description See Col. 5, Lines 9-27); a computing device (See Fig. 3, item 10) for assigning a modulator a modulator output value with to each of K states (See Figs. 1A-B, 3, items S, S+1, in description See Col. 5, Lines 9-27); and whereby modulator outputs a plurality of pulses according to modulator output value during each time period Pn (Tpwm) occurring within timer period Pt (T1 or T2), and whereby the resolution of n bit pulse width modulator equals n + log2(K) or 6 + log2(K) or 7 (See Fig. 1A, items Tc, T1, T2, S, S+1, Col. 5, Lines 8-27 and Col. 6, Lines 1-10).

Zuraski et al. does not show an additional timer to generate K associated states, wherein K is greater than 2.

Burgan et al. teaches an additional timer (counter) (See Fig. 11, item 1144, Col. 11, lines 51-65) to generate K associated states, wherein K is greater than 2 (See Fig. 12, items T0-T7, Col.12, Lines 9-18).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement (timer) counter as shown by Burgan et al. in Zuraski et al. apparatus and method in order to create an adaptive pulse-width modulator for pulse-width modulating a digital tone signal (See Col. 3, lines 60-64).

As to claim 11, Zuraski et al. teaches a computer program product for pulse width modulation comprising: a computer readable storage medium having computer readable program code embedded in medium (See Figs. 3-5, items 10, 501-509, in description See Col. 7, Lines 5-20), computer readable program code means having: a first computer instruction means for associating K timer states, wherein K is equal 2 (See Col. 6, Lines 1-10) with a timer having period Pt (T1 or T2) (See Fig. 1A-B, items T1, T2, in description See Col. 5, Lines 9-27); a second computer instruction means for reading a commanded pulse width modulation cycle (See Fig. 5, item 501, in description See Col. 7, Lines 22-30); a third computer instruction means for assigning a n bit modulator output with each one of K states according to the duty cycle (See Figs. 5-6, items 503, 601, in description See Col. 8, Lines 12-29).

Zuraski et al. does not show an additional timer to generate K associated states, wherein K is greater than 2.

Burgan et al. teaches an additional timer (counter) (See Fig. 11, item 1144, Col. 11, lines 51-65) to generate K associated states, wherein K is greater than 2 (See Fig. 12, items T0-T7, Col.12, Lines 9-18).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement (timer) counter as shown by Burgan et al. in Zuraski et al. apparatus and method in order to create an adaptive pulse-width modulator for pulse-width modulating a digital tone signal (See Col. 3, lines 60-64).

As to claim 12, Zurazki et al. teaches update n-bit modulator output value assigned to each state at time intervals of K*Pt equal to Tc = T1+T2 (See Fig. 1A, items Tc, T1, T2, Col. 5, Lines 24-27).

As to claims 2,6,16, Zuraski et al. teaches Pt is an integer multiple of Pn, since Tc and Tpwm are both derived from microprocessor clock (See Fig. 3, item 17, in description See Col. 3, Lines 33-40).

As to claims 4,8 Zuraski et al. teaches conventional case where Pt=Pn (T1=Tpwm without internal microprocessor timers) (See Figs. 1A-B, 3, in description See Col. 5, Lines 9-27).

As to claims 9,17, Zuraski et al. teaches Pt (T1) >> Pn (Tpwm) (See Figs.1A-B, items Tpwm and Tc, T1, T2).

Zuraski et al. does not show Pt is other than integer multiple of Pn. It would have been obvious to one of ordinary skill in the art at the time of the invention to use external clock to the timers of the microprocessor to have Pt other than integer multiple of Pn in the Zuraski et al. method.

As to claim 15, Zuraski et al. teaches timers are included within computing device (See Fig. 3, item 10, in description See Col. 3, Lines 30-36).

4. Claims 3, 7, 10, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable Zuraski et al. and Burgan et al. as aforementioned in claims 1, 5, 14 in view of Shibuya et al. (US Patent No. 6,191,868 B10)

Zuraski et al. and Burgan et al. do not show pulse width modulator includes an overflow bit.

Shibuya et al. teaches to truncate the overflow bit (See Fig. 2, item 17, in description See Col. 4, Lines 58-65).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the overflow approach as shown by Shibuya et al. in the Zuraski et al. and Burgan et al. method and apparatus in order to enhance the output resolution of PWM system.

Response to Amendment

5. Applicant's arguments filed on 10-17-03 with respect to claims 1-12, 14-19 have been considered but are moot in view of the new ground(s) of rejection.

Response to Arguments

6. Applicant's arguments filed on 10-17-03 with respect to claims 21-23 have been fully considered but they are not persuasive:

On page 5 of Argument, Applicant's stated that a hardware based pulse width modulator is clearly described starting on page 10, line 26. However, on page 11, Lines 9-10 nothing mentioned about hardware based pulse width modulator being hardware based. Contrary to that on Lines 15-18 the same page Applicant stated that computing device 920 may optionally include timer 918, which means that pulse width modulator is part of computing device as microprocessor and therefore not hardware based.

In the same paragraph and continue on the next page, Applicant's refers to page 5, stating that a specific reference to known hardware pulse width modulation is included. However, on page 5, Lines 19-21, Applicant stated that changing hardware in such fashion may be impractical which will lead to the page 11 of the Description, where computing device or microprocessor is shown as a practical solution.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

The Miller (US Patent No. 5, 023, 535) reference discloses high resolution pulse width modulation.

The Ma et al (Pub. No.: US 2002/0007467 A1) reference discloses microcontroller with a user configurable pulse width modulation.

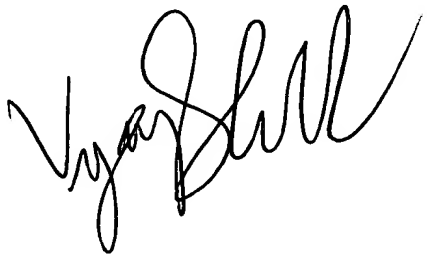
Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 703-305-5661. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ls 05-12-04



VIJAY SHANKAR
PRIMARY EXAMINER